

## What is Claimed is:

- [c1] A method of testing a semiconductor chip having a plurality of common I/Os associated therewith whose characteristics or properties may be tested by applying a test signal through a control I/O, the method comprising the steps of: performing a chip-to-package connectivity test upon at least one of the common I/O through the control I/O; and determining whether the common I/O is faulty from a result of the chip-to-package connectivity test.
- [c2] The method of claim 1, wherein performing a pin-to-package connectivity test comprises: launching a transition through the common I/O to an associated I/O package connection and pad; and observing a response of the transition.
- [c3] The method of claim 2, further comprising: triggering a first latch at an initialization of the transition response and triggering a second latch when the transition response has reached a transition threshold value.
- [c4] The method of claim 3, wherein determining whether the chip-to-package connection is faulty comprises: comparing a difference between values stored in association with the first and second latches.
- [c5] The method of claim 1, wherein determining whether the chip-to-package connection is faulty comprises: comparing a first RC constant associated with a first signal relating to a connectivity test of a first I/O with a second RC constant associated with a second signal relating to a connectivity test of a second I/O.
- [c6] The method of claim 5, further comprising identifying the first I/O as having a faulty connection if the first RC constant is greater than the second RC constant.
- [c7] The method of claim 1, wherein performing the chip-to-package connectivity test comprises generating a transition signal from a driver of the common I/O, wherein the driver is configured as a weak driver.

- [c8] The method of claim 7, wherein generating the transition from the weak driver comprises placing an additional impedance into connection with the driver prior to launching the transition.
- [c9] The method of claim 8, wherein placing an additional impedance into connection with the driver comprises placing a resistor into series connection with the driver.
- [c10] The method of claim 8, further comprising electrically shorting the additional impedance from connection with the driver after launching the transition.
- [c11] The method of claim 10, wherein electrically shorting the additional impedance includes completing a circuit around the additional impedance to bypass the additional impedance.
- [c12] A method of reduced pin count testing the chip-to-package connectivity of a semiconductor device, the method comprising: launching a transition from a common I/O driver on the packaged semiconductor device; observing a response of the transition at a point within the semiconductor device; determining whether a chip-to-package connection associated with the I/O is faulty from the response of the transition.
- [c13] The method of claim 12, further comprising driving the transition with a weak driver.
- [c14] An apparatus configured to launch a test signal to a common I/O of a semiconductor device from a driver on the semiconductor device which is associated with the common I/O using reduced pin count testing, the apparatus comprising: a test fixture configured to couple to a common I/O of the semiconductor device; a weak driver impedance coupled between the driver and the test fixture; wherein the apparatus is configured to launch the test signal through the weak driver impedance and the common I/O to the test fixture and evaluate a characteristic of a response to the test signal to determine whether a chip-to-package connection associated with the common I/O is faulty.

- [c15] The apparatus of claim 14, wherein the weak driver impedance includes at least one of a switchable impedance and a variable impedance.
- [c16] The apparatus of claim 14, wherein the weak driver impedance is an impedance having a resistive value of 1 K $\Omega$  or more.
- [c17] The apparatus of claim 16, wherein the weak driver impedance is approximately 10 K $\Omega$  or more.
- [c18] The apparatus of claim 14, further comprising a fixture impedance coupled between the test fixture and at least one of the semiconductor device and a potential relative to the semiconductor device.
- [c19] The apparatus of claim 18, wherein the fixture impedance comprises a capacitor coupled between the common I/O and a fixed potential relative to the semiconductor device.